REMARKS

Claims 22, 23, 25, 49, 50, 52, 56 and 58-62 are presently pending in this application. Claims 22, 23, 25, 49, 50, 52, 58 and 60 have been amended in this paper. No claims have been canceled in this paper. Thus, claims 22, 23, 25, 49, 50, 52, 56 and 58-60 are currently pending.

In the January 24, 2007 Office Action, claims 22, 23, 25, 49, 50, 52, 56 and 58-62 were rejected. More specifically, the pending claims were rejected as follows:

(A) Claims 22, 23 and 25 were rejected under 35 U.S.C. § 103(a) over the combination of Korean Patent No. 1997-0008549 to Kye et al. ("Kye") and U.S. Patent No. 5,348,033 to Levit ("Levit"); and

(B) Claims 49, 50, 52, 56 and 58-62 were rejected under 35 U.S.C. § 103(a) over the combination of Kye, Levit and U.S. Patent No. 6,413,150 to Blair ("Blair").

A. Response to the Section 103(a) Rejection over Kye and Levit

Claims 22, 23 and 25 were rejected under 35 U.S.C. § 103 over the combination of Kye and Levit. Claims 22, 23 and 25 have been amended to include subject matter that is similar to the subject matter of claim 56, which was not subject to this rejection. Claims 22, 23 and 25, more specifically, have been amended such that these methods further include "molding a protective casing around at least a portion of a die to form a package having a molded surface," and "before marking the molded surface, chemically etching at least a portion of the molded surface." Because claims 22, 23 and 25 include subject matter that is similar to subject matter included in claim 56, the rejection of claims 22, 23 and 25 over the combination of Kye and Levit should be withdrawn. The patentability of claims 22, 23 and 25 will be addressed below in the remarks directed toward the rejection of claim 56 over the combination of Kye, Levit and Blair.

B. Response to the Section 103(a) Rejection over Kye, Levit and Blair

Claims 49, 50, 52, 56 and 58-62 were rejected under 35 U.S.C. § 103 over the combination of Kye, Levit and Blair. The patentability of claims 22, 23, 25, 56, 60 and 62 will be addressed in one section, and the patentability of 49 will be addressed separately.

1. Claims 22, 23, 25, 56, 60 and 62

Independent claims 22, 23, 25, 56, 60 and 62 are directed toward various methods of packaging a microelectronic device (claims 56 and 62), finishing a surface of a protective package of a microelectronic device (claims 22, 23 and 25), and marking a surface of a protective resin package on a microelectronic device (claim 60). Methods for packaging microelectronic devices in accordance with claim 56 include molding a package compound at least partially around a microelectronic die in a mold to at least partially encase the microelectronic die such that a surface blemish is left on a marking surface of the mold compound. The method further includes removing the package from the mold, and etching at least a portion of the marking surface to remove a layer of material from the package "prior to marking the marking surface." The method continues by terminating the etching when the surface blemish has been at least partially removed from the package, and marking the etched marking surface after terminating the etching.

Several embodiments of methods in accordance with claim 56 are useful in many applications, and they are particularly useful for increasing the throughput of molding processes used to encase microelectronic dies with resins or other types of molding compounds. For example, resins can build up in the mold cavities after a period of use and leave asperities or stains on the molded surfaces of the package. (Specification, paragraph [0005].) When this happens, the molds must be cleaned and the packages may have a poor quality surface finish. (Specification, paragraph [0005].) As such, resin buildup in the mold cavities can reduce the throughput of molding machines and the yield of finish devices because the molds must be cleaned to provide a good marking surface before the devices are marked. Embodiments of methods in accordance with claim 56 can prolong the period between mold cleanings because the method removes surface asperities or stains before marking the surface with identifiers and/or

alignment fiducials such that problems associated with molding are resolved on the packages and not the in the mold.

Claim 56 is patentable over the combination of Kye, Levit and Blair because this combination of references fails to disclose or suggest all the features of this claim. For example, this combination of references fails to disclose or suggest "molding package compound at least partially around a microelectronic die in a mold to at least partially encase the microelectronic die" in combination with etching at least a portion of the marking surface "prior to marking the marking surface" and "marking the etched marking surface" after terminating the etching procedure. Kye merely teaches removing marks that have already been applied to the casing using a chemical removal agent, and then rinsing the casings to eliminate the residues of the markings removed by the chemical removal agent. In Kye, the chemical removal agent is used only after the casing has been marked; this is in direct contrast to etching the casing before it is marked. Levit further supports the order of the procedures set forth in Kye because Levit is directed toward an apparatus for transmitting parts along a path between processing stations in which the package devices are cleaned after existing marks applied to the casing have been removed. The combination of Kye, Levit and Blair accordingly fails to disclose or suggest the claimed combination of features of claim 56.

Claim 56 is further patentable over the combination of Kye, Levit and Blair because a person skilled in the art would not modify the method in Kye to come up with the combination of features set forth in claim 56. The prior art does not provide a reason to modify Kye to come up with claim 56 because the prior art does not recognize the problems addressed by methods in accordance with claim 56 or provide other benefits for making such a modification. As explained above, methods in accordance with claim 56 are useful for increasing the throughput of molding processes because they remove blemishes caused by the molding processes such that the mold does not need to be cleaned as often. None of the cited references recognizes this problem, and therefore these references do not provide a reason to modify Kye to come up with claim 56. The Examiner's reasoning in support of the rejection of claim 56 also does not provide a benefit for modifying the method of Kye to come up with the combination of features in claim 56. More specifically, the Examiner rejects claim 56 on the grounds that molding steps are conventional in

the art and it would have been obvious to mold a casing and remove the package from the mold in the method of Kye because these are conventional and useful techniques in the art. This reasoning misses the claimed feature of etching the casing before marking the casing. Moreover, irrespective of whether molding and removing procedures are known in the art, the applicants respectfully submit that it is not conventional to etch the marking surface created by the molding process before marking the marking surface with identification and/or alignment marks. In fact, modifying Kye to etch the die prior to marking the marking surface would merely add the costs and process time of another etching step to Kye's method without any apparent benefit provided by the prior art. The applicants accordingly request that the rejection of claim 56 under Section 103 over the combination of Kye, Levit and Blair be withdrawn.

Claims 22, 23, 25 and 62 include molding a protective casing around at least a portion of a die to form a package having a molded surface in combination with chemically etching at least a portion of the molded surface before marking the molded surface, and then marking the marking surface after cleaning residual materials and/or chemicals from the package. These features of claims 22, 23, 25 and 62 are similar to the features explained above with respect to claim 56. Claims 22, 23, 25 and 62 are accordingly patentable over the combination of Kye, Levit and Blair for reasons similar to those explained above with respect to claim 56. Claims 22, 23, 25 and 62 are further patentable over the cited combination of references because each of these independent claims includes additional features. For example, claim 22, 23 and 25 further include a cleaning procedure, and claim 25 still further includes a controlling procedure that controls the depth of the etching process. Claim 62 further includes molding the package compound such that a portion of the substrate remains exposed. In light of the foregoing, the applicants also respectfully request withdrawal of the rejection of claim 22, 23, 25 and 62 over the combination of Kye, Levit and Blair.

Claim 60 is also patentable over this combination of references. For example, neither Kye, Levit nor Blair discloses or suggests providing a plurality of unmarked microelectronic devices on a column substrate and simultaneously etching at least a portion of the surface of each package before marking the unmarked packages. As such, claim 60 is patentable over the

combination of Kye, Levit and Blair for reasons that are similar to those explained above with respect to claim 56.

2. Claim 49

Claim 49 is directed toward a method for simultaneously finishing a surface of a protective package on each of a plurality of microelectronic devices carried on a common substrate. Embodiments of this method include molding a plurality of protective casings around at least a portion of a plurality of individual dies to form a plurality of individual packages having molded surfaces. The method further includes etching at least a portion of the molded surface of individual packages to remove a layer of material from the packages before marking the molded surfaces, and then cleaning residual materials and/or chemicals from the packages after terminating the etching of the package surfaces. This method further includes marking the etched surfaces of the packages after cleaning, and cutting the common substrate to separate the microelectronic devices from one another after terminating the etching.

Claim 49 is patentable under Section 103 over the combination of Kye, Levit and Blair because this reference fails to disclose or suggest several features of claim 49. For example, these references fail to disclose or suggest the combination of molding a protective casing around at least a portion of a plurality of dies, etching at least a portion of the molded surface of individual packages before marking the molded surfaces, and then marking the etched surfaces of the packages. Claim 49 is further patentable over this combination of references because none of the references discloses simultaneously finishing the surface of each of a plurality of microelectronic devices on a common substrate by etching the surfaces. The applicants, therefore, respectfully request withdrawal of the rejection of claim 49 over the combination of Kye, Levit and Blair.

Conclusion

In view of the foregoing, the pending claims comply with 35 U.S.C. § 112 and are patentable over the applied art. The applicants accordingly request reconsideration of the application and respectfully submit that the pending claims are in condition for allowance. If the

Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to contact Paul Parker at (206) 359-3258.

Respectfully submitted,
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